What is claimed is:

1. A data transfer control system for data transfer through a bus, the data transfer control system comprising:

an address storage section which stores a first address, the first address being stored in a page table element that is being processed at a point at which a bus reset occurs among page table elements of a page table specified by a first command packet transferred through a first bus;

an address comparison section which reads out a second address and compares the stored first address and the read-out second address, the second address being stored in a page table element having the same element number as the page table element in which the first address is stored among page table elements of a page table specified by a second command packet, when the second command packet is transferred through the first bus after the bus reset occurs; and

a transfer restart section which restarts data transfer from the page table element that is being processed at the point at which the bus reset occurs, when it has been determined that the first address and the second address are the same.

2. The data transfer control system as defined by claim 1, wherein:

the address storage section stores a first direct address which is specified by the first command packet when a page table is absent;

the address comparison section compares the first direct address and a second direct address which is specified directly by the second command packet when a page table is absent; and

the transfer restart section restarts the data transfer when it has been determined that the first direct address and the second direct address are the same.

3. The data transfer control system as defined by claim 1, wherein:

the address storage section stores K first addresses (where K is an integer equal to or greater than two) which are stored in K page table elements among the page table elements of the page table specified by the first command packet, the K page table elements including consecutive page table elements starting from an initial page table element to the page table element that is being processed at the point at which the bus reset occurs;

the address comparison section reads out K second addresses which are stored in page table elements having the same element numbers as the page table elements in which the first addresses are stored among the page table elements of the page table specified by the second command packet transferred in after the bus reset occurs, and compares the stored K first addresses and the read-out K second addresses; and

the transfer restart section restarts the data transfer from the page table element that is being processed at the point at which the bus reset occurs, when it has been determined that the K first addresses and K second addresses are the same.

4. A data transfer control system for data transfer through a bus, the data transfer control system comprising:

a command storage section which stores a content of a first command packet transferred through a first bus;

an address storage section which stores a first direct address which is specified directly by the first command packet, when a page table is absent;

a command comparison section which compares a content of the first command packet and a content of a second command packet, when the second command packet is transferred through the first bus after a bus reset occurs;

an address comparison section which compares a first direct address which is specified directly by the first command packet and a second direct address which is specified directly by the second command packet, when the page table is absent; and

a transfer restart section which restarts data transfer as a resumption of data transfer at a point at which the bus reset occurs on condition that it has been determined that the contents of the first and second command packets are the same and also that the first and second direct addresses are the same when the page table is absent, and restarts data transfer as a resumption of data transfer at the point at which the bus reset occurred on condition that it has been determined that the contents of the first and second command packets are the same when the page table is present.

5. The data transfer control system as defined by claim 1, further comprising:

a command processing section which receives a command packet transferred through the first bus, issues a command indicated by the command packet to a device connected to a second bus, and instructs a start of DMA transfer through the second bus; and

a command abort section which aborts the command issued to the device connected to the second bus based on the first command packet, after DMA transfer started based on the first command packet has been completed, when data transfer is not be restarted by the transfer restart section.

6. The data transfer control system as defined by claim 4, further comprising:

a command processing section which receives a command packet transferred through the first bus, issues a command indicated by the command packet to a device connected to a second bus, and instructs a start of DMA transfer through the second bus; and

a command abort section which aborts the command issued to the device connected to the second bus based on the first command packet, after DMA transfer started based on the first command packet has been completed, when data transfer is not be restarted by the transfer restart section.

7. The data transfer control system as defined by claim 5,

wherein the command abort section controls dummy data transfer to or from the device connected to the second bus until the DMA transfer is complete.

8. The data transfer control system as defined by claim 6,

wherein the command abort section controls dummy data transfer to or from the device connected to the second bus until the DMA transfer is complete.

9. The data transfer control system as defined by claim 7,

wherein the command abort section aborts the command without controlling the dummy data transfer, in a case that DMA transfer is not operating when it is determined whether or not the command is to be aborted.

10. The data transfer control system as defined by claim 8,

wherein the command abort section aborts the command without controlling the dummy data transfer, in a case that DMA transfer is not operating when it is determined whether or not the command is to be aborted.

11. The data transfer control system as defined by claim 7, further comprising:

a pointer management section which manages pointers of a packet buffer that temporarily stores transfer data, by a ring buffer method, updates a first pointer every

time transfer data from the second bus is written to the packet buffer, and updates a second pointer every time transfer data to the first bus is read out from the packet buffer,

wherein the command abort section controls the dummy data transfer by performing a dummy update of the second pointer in such a manner that the second pointer is not overtaken by the first pointer that is updated every time transfer data from the second bus is written to the packet buffer.

12. The data transfer control system as defined by claim 8, further comprising:

a pointer management section which manages pointers of a packet buffer that temporarily stores transfer data, by a ring buffer method, updates a first pointer every time transfer data from the second bus is written to the packet buffer, and updates a second pointer every time transfer data to the first bus is read out from the packet buffer,

wherein the command abort section controls the dummy data transfer by performing a dummy update of the second pointer in such a manner that the second pointer is not overtaken by the first pointer that is updated every time transfer data from the second bus is written to the packet buffer.

13. The data transfer control system as defined by claim 7, further comprising:

a pointer management section which manages pointers of a packet buffer that temporarily stores transfer data, by a ring buffer method, updates a third pointer every time transfer data to the second bus is read out from the packet buffer, and updates a fourth pointer every time transfer data from the first bus is written to the packet buffer,

wherein the command abort section controls the dummy data transfer by performing a dummy update of the fourth pointer in such a manner that the fourth pointer is not overtaken by the third pointer that is updated every time transfer data to the second bus is read out from the packet buffer.

14. The data transfer control system as defined by claim 8, further comprising:

a pointer management section which manages pointers of a packet buffer that temporarily stores transfer data, by a ring buffer method, updates a third pointer every time transfer data to the second bus is read out from the packet buffer, and updates a fourth pointer every time transfer data from the first bus is written to the packet buffer,

wherein the command abort section controls the dummy data transfer by performing a dummy update of the fourth pointer in such a manner that the fourth pointer is not overtaken by the third pointer that is updated every time transfer data to the second bus is read out from the packet buffer.

15. The data transfer control system as defined by claim 1,

wherein the first bus is a bus in which data transfer is performed by the IEEE 1394 standard.

16. The data transfer control system as defined by claim 4,

wherein the first bus is a bus in which data transfer is performed by the IEEE 1394 standard.

17. An electronic instrument comprising:

the data transfer control system as defined in claim 1; and

a device connected to a second bus of the data transfer control system.

18. An electronic instrument comprising:

the data transfer control system as defined in claim 4; and

a device connected to a second bus of the data transfer control system.

19. A data transfer control method for performing data transfer through a bus, the method comprising:

storing a first address, the first address being stored in a page table element that is being processed at a point at which a bus reset occurs among page table elements of a page table specified by a first command packet transferred through a first bus;

reading out a second address and comparing the stored first address and the read-out second address, the second address being stored in a page table element having the same element number as the page table element in which the first address is stored among page table elements of a page table specified by a second command packet, when the second command packet is transferred through the first bus after the bus reset occurs; and

restarting data transfer from the page table element that is being processed at the point at which the bus reset occurs, when it has been determined that the first address and the second address are the same.

20. A data transfer control method for performing data transfer through a bus, the method comprising:

storing a content of a first command packet transferred through a first bus;

storing a first direct address which is specified directly by the first command packet, when a page table is absent;

comparing a content of the first command packet and a content of a second command packet, when the second command packet is transferred through the first bus after a bus reset occurs;

comparing a first direct address which is specified directly by the first command packet and a second direct address which is specified directly by the second command packet, when the page table is absent;

restarting data transfer as a resumption of data transfer at a point at which the bus reset occurs on condition that it has been determined that the contents of the first and second command packets are the same and also that the first and second direct addresses are the same when the page table is absent; and

restarting data transfer as a resumption of data transfer at the point at which the bus reset occurred on condition that it has been determined that the contents of the first and second command packets are the same when the page table is present.